REMARKS

The application has been carefully reviewed in light of the Office Action dated September 10, 2002. Applicant gratefully acknowledges the Examiner's statement that claims 2, 4-12, 15, 16, 18-21, 24, 26-34, 37, 38, 40-43, 47, 48 and 50-53 contain allowable subject matter. Claims 1, 4, 8, 13, 35, 45 and 52 have been amended. Claims 2 and 3 have been cancelled. Claims 55-58 have been newly added. Claims 1 and 4-58 are now pending in this case.

Claims 52 and 53 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claim 52 has been amended to correct the indefiniteness and both claims 52 and 53 are in compliance with 35 U.S.C. § 112.

Claims 1, 3, 13, 14, 17, 22, 23, 25, 35, 36, 39, 44-46, 49 and 54 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yee et al. (U.S. Patent No. 5,638,529) and Leung (U.S. Patent No. 6,415,353). Applicant respectfully traverses the rejection and requests reconsideration.

Claim 1 has been amended to include the allowable subject matter of cancelled claim 2. Claim 1 is now in condition for allowance.

Claims 13, 35 and 45 have been amended so that they now recite "a communication link for delivering data access commands to said DRAM on predetermined time slots." [Emphasis added.] As acknowledged by the Office Action, none of the cited references teach or suggest that a data access command is delivered to the DRAM on predetermined time slots, much less such a configuration as included in the respective inventive combinations defined by claims 13, 35 and 45.

Claims 4-12, 14-34, 36-44 and 46-54 depend from claims 1, 13, 35 and 45, and are allowable at least for those reasons discussed above, and also because none of the cited references teach or suggest their respective inventive combinations.

Newly added claim 55 recites "assigning predetermined time slots during which a data access command may be placed on a command/address bus; and performing a non-conflicting refresh operation during a period of time between said predetermined time slots."

Newly added claims 56-58 recite "a communication link for delivering data access commands to [a] DRAM on predetermined time slots; and . . . performing a non-conflicting refresh on said memory cells during a time interval between said predetermined time slots."

Claims 55-58 are allowable since none of the cited references teach or suggest the inventive combinations respectively defined by claims 55-58.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejections of the claims and to pass this application to issue.

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Respectfully submitted,

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1. (Amended) A method for refreshing memory cells, comprising:

determining that a refresh of said memory cells is required;

determining that a data access [is desired] command has been applied to a command/address bus at a first predetermined time slot; and

initiating said refresh [at a predetermined] during a time period between said first predetermined time slot and a second predetermined time slot without delaying said data access.

4. (Amended) The method of claim [2] 1 further comprising determining whether said data access command conflicts with said refresh.

8. (Amended) The method of claim 7 further comprising:

determining that a second data access command has been applied to said command/address bus at said [predetermined] next available time slot; and

determining whether said second data access command conflicts with said refresh.

13. (Amended) A system for refreshing memory cells of a dynamic random access memory (DRAM) comprising:

a memory array containing said memory cells;

a communication link for delivering data access commands to said DRAM on predetermined time slots; and

a controller for operating said memory array in accordance with said data access commands, wherein

said controller is configured to determine that said memory cells require a refresh, and wherein

said controller is configured to initiate said refresh at a predetermined time and without delaying a data access triggered by a data access command.

35. (Amended) An integrated circuit semiconductor device containing a system for refreshing memory cells of a dynamic random access memory (DRAM), said integrated circuit semiconductor device comprising:

a memory array containing said memory cells;

a communication link for delivering data access commands to said DRAM on predetermined time slots; and

a controller for operating said memory array in accordance with said data access commands, wherein

said controller is configured to determine that said memory cells require a refresh, and wherein

said controller is configured to initiate said refresh at a predetermined time and without delaying a data access triggered by a data access command.

45. (Amended) A processor-based system, comprising:

a processor; and

a dynamic random access memory (DRAM) coupled to said processor, said dynamic random access memory having a system for refreshing memory cells in said dynamic random access memory, said system comprising:

a memory array containing said memory cells;

a communication link for delivering data access commands to said DRAM on predetermined time slots; and

a controller for operating said memory array in accordance with said data access commands, wherein

said controller is configured to determine that said memory cells require a refresh, and wherein

said controller is configured to initiate said refresh at a predetermined time and without delaying a data access triggered by a data access command.

52. (Amended) The processor-based system of claim [45] 51, wherein said predetermined edge is defined as every fourth positive edge of a dynamic random access memory (DRAM) input clock.